REMARKS

Claims 1 – 35 are pending in the Application, of which claims 8-12 and 19-35 are withdrawn from consideration.

RESPONSE TO ARGUMENTS

The present Office Action alleges the Applicants argued the references individually. Applicants respectfully disagree and respectfully direct attention to page 12 lines 5 – 7 of the previous response in which Applicants respectfully asserted that the present invention is neither shown nor suggested by the Cheng et al. nor the Potts references, alone ***or together in combination***. In addition, the previous response [page 13 lines 1 - 4] reiterated the ***Office Action acknowledgement*** that the ***Cheng*** reference ***does not teach*** a test signal redistribution trace is disposed such that multiple test signals are accessible at varying degrees of electronic component granularity within the die along a test signal redistribution layer trace. The previous response went on to indicate that Applicants respectfully assert the ***Potts reference does not overcome*** these and ***other shortcomings of the Cheng reference***. Applicants respectfully assert that Applicants argued against the references in combination by addressing an element that the Office Action even acknowledges the Cheng reference does not

teach and going on to explain why Applicants respectfully assert the Potts reference also does not teach the element.

The present Office Action acknowledges that the Cheng reference does not teach [page 3 lines 15 – 19] a test signal redistribution trace is disposed such that multiple test signals are accessible at varying degrees of electronic component granularity within the die along a test signal redistribution layer trace. In the remarks section, the present Office Action appears to allege that Potts shows multiple test signals CP1.4, CP2.4 and CP3.4 are accessible at varying degrees of electronic component granularity via SP1, SP2 and SP3 within a die and along a test signal redistribution layer trace 62. To the extent the Potts reference may show a shared pad SP1, SP2 and SP3 [Figure 3] and may show SPx, CPa and CPb [Figure 4] are accessing two transistors 42a and 42b of ***similar component granularity*** [Figure 4], Applicants respectfully assert the Potts reference does not teach multiple test signals are accessible at ***varying degrees*** of electronic ***component granularity***. Applicant respectfully asserts that to the extent the Potts reference may show accessing two transistors 42a and 42b of ***similar component granularity*** it does not teach multiple test signals are accessible at ***varying degrees*** of electronic ***component granularity***.

In addition, to the extent the Potts reference may mention the preferred embodiments contemplate the inclusion of various structures including SP1, SP2, SP3 and SPx and portions of layer 62 within *scribe area* 34 that is ***not part of the die*** [Figure 3 and Figure 4] and the scribe area is destroyed [Paragraph 21], Applicants respectfully assert the Potts reference ***teaches away*** from a semiconductor ***die comprising*** a conductive test signal bump and a test signal redistribution layer trace for communicating the test signals to the conductive test signal bump, wherein the test signal redistribution trace is included in a redistribution layer and the test signal redistribution trace is disposed such that multiple test signals are accessible at varying degrees of electronic component granularity within the die and along the test signal redistribution layer trace, the test signal redistribution layer trace communicatively coupled to the conductive test signal bump.

103 REJECTIONS

The present Office Action indicates Claims 1 and 3 – 7 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Cheng et al. (US Patent No. 6,686,615) in view of Potts (US 2003/0124816). Applicants respectfully assert that the present invention is neither shown nor suggested by the Cheng et al. reference nor the Potts reference, alone or together in combination.

Applicants respectfully assert that the Cheng et al. reference is not directed to the present invention as recited in Claim 1. Specifically the present invention, as set forth in independent Claim 1 recites in part:

> ... said test signal redistribution trace is disposed such that multiple test signals are accessible at varying degrees of electronic component granularity within said die and along said test signal redistribution layer trace ... .

The present Office Action acknowledges the Cheng reference does not teach a test signal redistribution trace is disposed such that multiple test signals are accessible at varying degrees of electronic component granularity within the die along a test signal redistribution layer trace. Applicants respectfully assert the Potts reference does not overcome these and other shortcomings of the Cheng et al. reference.

To the extent Potts reference may mention and show the transistors 42a and 42b on *two different* die 32a and 32b [Figure 4, Paragraphs 0024 and 0027], Applicants respectfully asserts the Potts reference does not teach that multiple test signals are accessible at varying degrees of electronic component granularity *within said die* and along said test signal redistribution layer trace. In addition,

to the extent the Potts reference shows accessing two transistors 42a and 42b of *similar component granularity* of [Figure 4], Applicants respectfully assert the Potts reference does not teach multiple test signals are accessible at *varying degrees* of electronic *component granularity*. Furthermore, to the extent the Potts reference may mention the preferred embodiments contemplate the inclusion of various structures including SPx and portions of layer 62 within *scribe area* 34 which are destroyed [Figure 4 and Paragraph 21], Applicants respectfully assert the Potts reference teaches away from a semiconductor *die comprising* a conductive test signal bump.

Applicants respectfully assert Claims 2 - 7 are allowable as depending from allowable independent Claim 1.

With respect to Claim 6, to the extent the Cheng et al. reference may show a redistribution trace that has a partial bend [Figure 2], Applicants respectfully assert the Cheng et al. reference does not teach a spiral pattern. Applicants respectfully assert for example the spiral pattern can run in a circular pattern while receding from or approaching a point or center.

The present Office Action indicates Claims 13, 14 and 18 are is rejected under 35 U.S.C. 103 (a) as being unpatentable over Lin (US Patent No. 5,258,648) in view of Potts (US 2003/0124816). Applicants respectfully assert that the present invention is neither shown nor suggested by the Lin nor the Potts references, alone or together in combination.

Applicants respectfully assert that the Lin reference is not directed to the present invention as recited in Claim 13. Specifically the present invention, as set forth in independent Claim 13 recites in part:

> ...a conductive trace disposed such that multiple test signals are accessible at varying degrees of electronic component granularity within said package substrate and along said conductive trace ... .

The present Office Action acknowledges the Lin reference does not teach test signal redistribution trace is disposed such that multiple test signals are accessible at varying degrees of electronic component granularity within the package substrate and along a test signal redistribution layer trace. Applicants respectfully assert the Potts reference does not overcome these and other shortcomings of the Lin reference.

To the extent Potts reference may mention and show the transistors 42a and 42b on *two different* die 32a and 32b [Figure 4, Paragraph 0024 and 0027], Applicants respectfully asserts the Potts reference does not teach that multiple test signals are accessible at varying degrees of electronic component granularity *within said die* and along said test signal redistribution layer trace. In addition, to the extent the Potts reference shows accessing two *components of similar granularity* of transistors 42a and 42b [Figure 4], Applicants respectfully assert the Potts reference does not teach multiple test signals are accessible at *varying degrees* of electronic *component granularity*. Furthermore, to the extent the Potts reference may mention the preferred embodiments contemplate the inclusion of various structures including SPx and portions of layer 62 within *scribe area* 34 which are destroyed [Figure 4 and Paragraph 21], Applicants respectfully assert the Potts reference teaches away from a package substrate for communicating test signals on an external access point.

Applicants respectfully assert Claims 14 – 18 are allowable as depending from allowable independent Claim 13.

The present Office Action indicates Claim 2 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Cheng et al. and Potts and further in view of Lin.

Applicants respectfully assert that the present invention is neither shown nor suggested by the Cheng et al., the Potts nor the Lin references, alone or together in combination.

Applicants respectfully reassert that Claim 2 is allowable as depending from an allowable independent Claim 1 as argued above. The present Office Action acknowledges that the Cheng et al. reference fails to teach the conductive bump being electrically coupled to a test signal access component of a package substrate and also acknowledges the Potts reference also does not teach the same. Applicants respectfully assert that the Lin reference does not overcome these and other shortcomings of the Cheng et al. and or Potts references alone or together in combination.

To the extent the Lin reference may show a trace on Figure 5 and may mention an electrical connection between the test connection and via [Col. 7 lines 10 - 27], Applicants respectfully assert the Lin et al. reference does not teach the conductive traces are disposed such that multiple test signals are accessible at varying degrees of electronic component granularity.

The present Office Action indicates Claims 15 - 17 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Lin and Potts in view of Cheng et al. Applicants respectfully assert that the present invention is neither shown nor suggested by the Cheng et al., the Potts, nor the Lin references, alone or together in combination.

With regards to Claims 15-17 the present Office Action acknowledges the Lin reference fails to disclose a semiconductor die comprising a test signal redistribution layer comprising conductive traces; a test probe point for accessing signals in said semiconductor die and for electrical coupling to said test signal redistribution layer; a test access via for electrically coupling said test probe point to said test signal redistribution layer; and a conductive bump for conveying a test signal off of said semiconductor die to said package substrate, said conductive bump located on a first surface of said semiconductor die and electrically coupled to said test signal redistribution layer. Applicant respectfully asserts the Cheng and Potts references do not overcome these and other shortcomings of the Lin reference.

To the extent the Potts reference may mention the preferred embodiments contemplate the inclusion of various structures including SPx and portions of

layer 62 within *scribe area* 34 which are destroyed [Figure 4 and Paragraph 21], Applicants respectfully assert the Potts reference teaches away from a semiconductor *die comprising* a conductive test signal bump.

The present Office Action also acknowledges the Lin and Potts reference further do not disclose a conductive bump for conveying a test signal off of said semiconductor die to said package substrate, said conductive bump located on a first surface of said semiconductor die and electrically coupled to said test signal redistribution layer routing of said test signal redistribution layer conductive traces is such that trace widths and spacing is a minimum without causing signal interference. Applicants respectfully assert the Cheng et al. reference does not overcome these and other shortcomings of the Lin reference.

As set forth above Applicants respectfully assert the Cheng et al. reference does not teach the conductive traces are disposed such that multiple test signals are accessible at varying degrees of electronic component granularity. The present Office Action alleges Cheng et al. appears to disclose in FIG 2 test signal redistribution layer conductive traces 21 are routed such that trace widths and spacing is a minimum

without causing signal interference. To the extent the Cheng et al. reference may show traces [Figure 2], Applicants respectfully assert the Cheng et al. reference does not teach routing of test signal redistribution layer conductive traces is such that trace widths and spacing is a minimum without causing signal interference.

The present Office Action also alleges the Cheng reference teaches conductive bump 40 for conveying a test signal off of said semiconductor die 10 inherently to a package substrate. Anticipation by inherent disclosure is appropriate only when the references disclose prior art that must ***necessarily*** (emphasis added) include the unstated limitation. See Transclean Corp. v. Bridgewood Services Inc., 290 F3.d 1364, 1373, 62 USPQ2d 1865 (Fed Cir. 2002). Applicants respectfully assert that the possibility or even probability is not enough. See Motorola, Inc. v. Interdigital Technology Corp. 930 F. Supp. 952, 970 (D. Del. 1996). Applicants respectfully assert that the Chen et al. reference does ***not necessarily*** (emphasis added) teach a test signal off of said semiconductor die to a package substrate. Applicants respectfully assert the Potts reference even mentions a useful testing mechanism for some devices that is used for testing and then presumably much if not all of the testing structure is required to be removed before the integrated circuit die is usually in a circuit

package or the like [Paragraph 8]. Applicants respectfully assert the Potts reference indicates at least one situation in which the Chen et al. reference does ***not necessarily*** (emphasis added) teach a test signal off of said semiconductor die to a package substrate.

CONCLUSION

In light of the above-listed amendments and remarks, Applicant respectfully request allowance of the remaining Claims. The examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application. Applicant respectfully petitions for a 1 Month extension of time under 37 C.F.R. 1.136 and is including the fee under 37 C.F.R. 1.17. If an additional extension of time is required, please consider this a petition therefore. Please charge and additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,
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